IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An apparatus comprising:

one or more Input/Output (I/O) conductors, wherein the I/O conductors pass through a hermetic seal such that a first end of the I/O conductors resides on a non-hermetic side of the hermetic seal and a second end of the I/O conductors resides on a hermetic side of the hermetic seal within a hermetically sealed interior of a hermetically sealed metal case of the apparatus;

a printed circuit interconnect substrate residing on the hermetic side of the hermetic seal, wherein the printed circuit interconnect substrate includes a multi-layer circuit board comprising a buried signal layer between first and second conductive layers, wherein each conductive layer is electrically connected to a constant voltage to form a constant voltage plane, wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors to provide electrical shielding, and wherein one I/O conductor provides an electrical connection to the constant voltage plane; and

one or more ceramic chip capacitors mounted on the printed circuit interconnect substrate ~~to face inward into~~ and mounted within the hermetically sealed interior of the hermetically sealed metal case, wherein a first end of each capacitor is electrically connected via printed circuit interconnect to the second end of an I/O conductor and a second end of each capacitor is electrically connected via the printed circuit interconnect to the metal case.

2. (Original) The apparatus of claim 1, wherein the printed circuit interconnect substrate is mounted on the hermetic side of the hermetic seal.

3. (Original) The apparatus of claim 1, wherein the printed circuit interconnect substrate includes a printed circuit board material.

4. (Original) The apparatus of claim 3, wherein the printed circuit board material includes a ceramic.

5. (Original) The apparatus of claim 3, wherein the printed circuit board material includes FR4.

6. (Previously Presented) The apparatus of claim 1, wherein the printed circuit interconnect substrate includes flexible circuit tape.

7. (Previously Presented) The apparatus of claim 6, wherein the flexible circuit tape includes polyimide.

8. (Original) The apparatus of claim 1, wherein the printed circuit interconnect substrate is a multi-layer substrate.

9. (Original) The apparatus of claim 1, wherein the printed circuit interconnect substrate includes an electrically conductive medium.

10. (Original) The apparatus of claim 9, wherein the electrically conductive medium includes solder.

11. (Original) The apparatus of claim 9, wherein the electrically conductive medium includes conductive epoxy.

12. (Original) The apparatus of claim 9, wherein the electrically conductive medium includes wire-bonds.

13. (Original) The apparatus of claim 1, wherein the capacitors have a dielectric breakdown voltage of about 1200 volts.

14. (Original) The apparatus of claim 1, wherein the capacitors have a dielectric breakdown voltage within a range of about 200 to 1500 volts.

15. (Original) The apparatus of claim 1, wherein the capacitors are discrete capacitors.

16. (Original) The apparatus of claim 15, wherein the capacitors include surface mount packaging.

17. (Original) The apparatus of claim 1, wherein the capacitors are included in a multi-chip package.

18. (Original) The apparatus of claim 1, wherein the capacitors are adapted to filter electromagnetic interference.

19. (Original) The apparatus of claim 1, wherein the hermetic seal is part of an implantable medical device.

20. (Original) The apparatus of claim 19, wherein the hermetic seal includes a ceramic.

21. (Original) The apparatus of claim 19, wherein the hermetic seal includes an epoxy.

22. (Original) The apparatus of claim 19, wherein the hermetic seal includes a glass.

23. (Original) The apparatus of claim 1, wherein the I/O conductors are pins.

24. (Original) The apparatus of claim 1 wherein the I/O conductors are wires.

25. (Original) The apparatus of claim 1 wherein the I/O conductors are conductive traces.

26. (Original) The apparatus of claim 25, wherein the conductive traces are included in a printed circuit interconnect that accommodates surface mounting of electronic components.

27-37. (Canceled)